Segundero

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Laboratory exercise number:

2nd Partial Exam

Laboratory exercise name:

Segundero

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| Names: | Roll Number | Date |
| Javier Mondragón M. | A01365137 | 25/October/2019 |

Lab description:

The purpose of this laboratory is to learn how program an FPGA using VHDL using the skills learnt in class. Recycling the code from previous labs, the implementation of the clocks using the one inside the FPGA the project must be a counter from a desired time to 0.

The material used was:

Nexys 3 by Digilent for the FPGA

ISE Project Naviator for the VHDL compiler and editor

Adept by Digilent for the deployment to the FPGA

Schematics, block diagrams and/or timing diagrams:

The following table shows the behavior of the counter, Q being the counter. The enable is just set to 1 every time the 100MHz clock reach it’s limit. Every time Q reach 0, a led will turn on indicating the count has reach its limit.

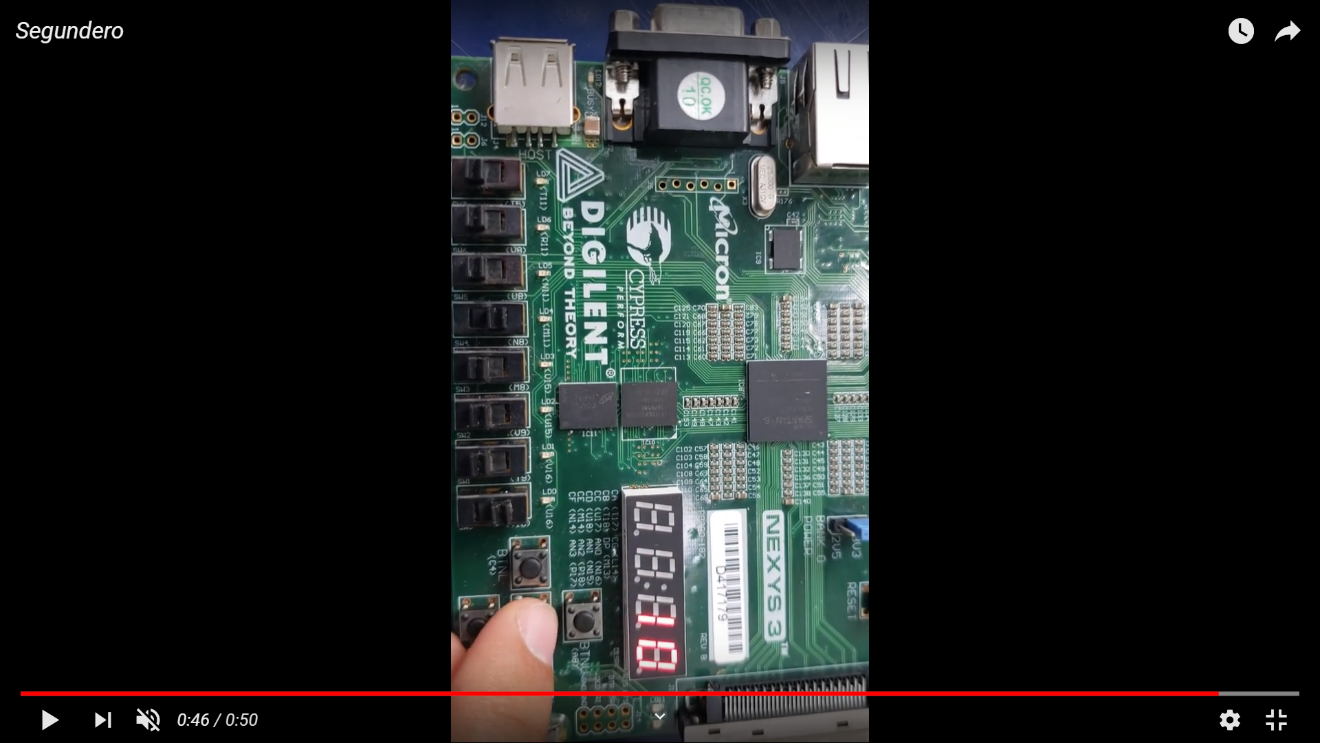
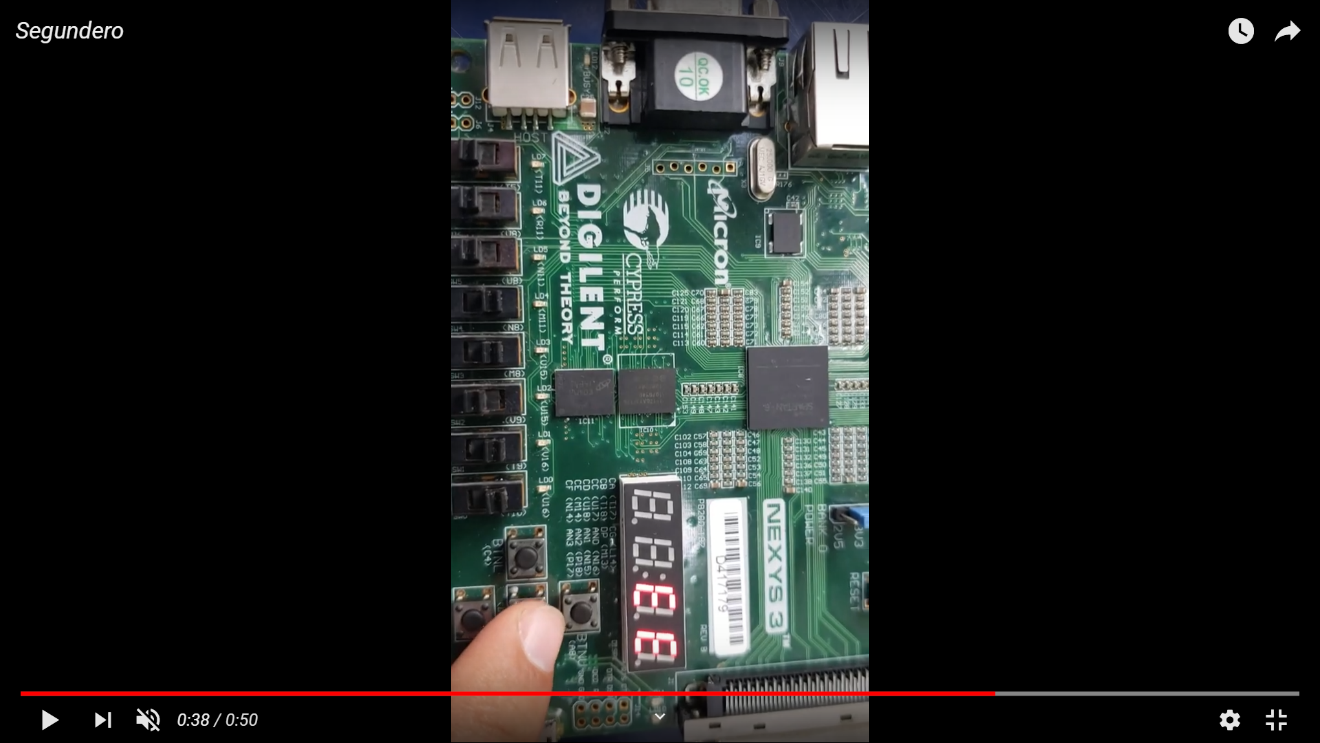
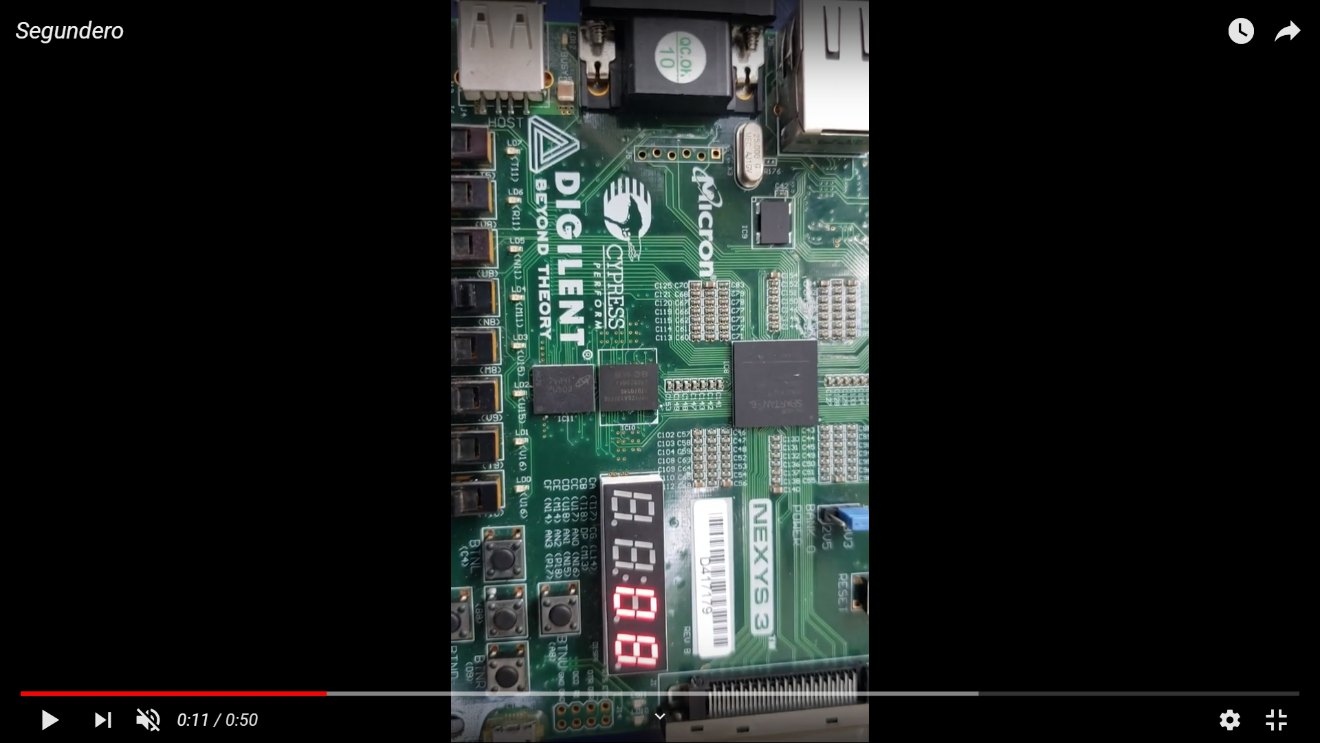
|  |  |  |  |
| --- | --- | --- | --- |
| Clk1Hz | Enable | Rst | Q |
| X | X | 1 | 0 |
| 0 | 0 | 0 | Q |
| ↑ | 0 | 0 | Q |
| ↑ | 1 | 0 | Q-1 |

Results obtained:

The result was a successful timer from a desired count to 0. In case of an invalid value, the display will show EE.

Evidence:

Video: https://youtu.be/MhLGeLHOTJs



Conclusions:

The timer was a difficult task for one and a half hour, the task for me and my partner Alejandro Tamayo was difficult because of time pressure but the ideas were executed correctly.

Problems encountered:

The most difficult problems was the time pressure.